

The background of the entire page is a close-up, high-angle photograph of a blue printed circuit board (PCB). The board is densely packed with white conductive traces and various electronic components, including several integrated circuits (chips) and smaller surface-mount components. The lighting is dramatic, highlighting the textures of the components and the intricate patterns of the circuitry. In the top left corner, there is a white rectangular box containing the Siemens logo and tagline. In the center, there is a dark blue rectangular box with white text. In the bottom right, there is a large teal-to-blue gradient box containing the main title and subtitle. At the very bottom, there is a white area with the authors' names and the Siemens website URL.

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Thermal characterization of complex electronics: A basic primer on structure functions

Mechanical analysis

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Evolution of power, size and temperature in electronics design

The major cause of system breakdown used to be overheating of critical components. At the hottest points in some of these systems, semiconductor junctions can reach 150°C or more, getting very close to the limits of their operation. These high temperatures will modify and eventually destroy the circuit operation unless excess heat is removed from the chip. But failure analysis shows that in today's system designs, this is not the only problem.

Typical component breakdown can also be caused by repeated thermal transients. Heating and cooling induces shear stresses at the material interfaces in the package structure (die attach, solder joint), which result in delamination, tear off, etc. The lack of heat removal through the resulting diminished contact area can cause thermal runaway.

Cooling is a 3D effect

For a long time, packaged electronic components were represented by a single thermal resistance in the datasheet. Power devices were usually encapsulated in packages with a dedicated cooling surface, called the "case." In discrete semiconductors (diodes, transistors), the hottest portion of the device was the pn-junction. As a first estimation, the engineer accepted that the temperature rise of the junction above the surface on which the package was mounted was the supplied thermal resistance multiplied by the applied power.

In conventional electronics as well as in solid-state lighting, the junction temperature (T_j) is a primary quantity that influences system reliability and lifetime. The junction temperature of an LED is a performance indicator of the thermal design, and many properties of the light output of an LED depend on the absolute junction temperature.

Single thermal resistance values such as the junction-to-case (R_{thJC}) are still part of datasheets used for component selection and in the early design phase. However, the complex three-dimensional nature of the cooling can only be predicted using sophisticated simulation tools that are combined with thermal measurements.

The thermal transient measurement method was developed to address these issues, providing a better solution than using thermal sensors. Today, accurate thermal characterization is needed to be able to create an optimal design for electronic systems. Thermal characterization techniques help to provide better results when developing models for simulation. Using the combination of thermal characterization, thermal transient testing and 3D thermal modeling saves time and costs by reducing the need for iterations of physical prototypes, re-spins during production and recalls of defective products from the field.

At its basic level, thermal transient testing means applying a steady, low power level to the device and then instantly switching to a higher level to observe a heating transient. Similarly, switching from a higher power level to a lower one, the cooling of the device can be monitored. These transients can be completely captured until the steady state is reached. For many more details on the math, theory and techniques behind the development of thermal transient testing techniques from this base point to what is commonly used today, see the book *Thermal Management for LED Applications*¹, and the appendix at the end of this whitepaper.

Structure functions: A revolution of interpretation

The development of thermal transient measurements for model creation has culminated in the Cauer-ladder network model. This model is useful for associating circuit elements with physical regions. The behavior described by the model is the basis for identifying the heat-flow path using “structure functions.” Researchers at the University of Budapest developed structure-function analysis methods to fulfill the need for greater interpretation inside packages². Methods for thermal testing of packaged semiconductor devices were introduced by Székely³, and they have radically changed the interpretation of thermal measurements. As a result, the Simcenter T3STER™ thermal transient analysis software system was created.

Structure functions transform the thermal transient measurement result into a thermal resistance versus thermal capacitance profile, which provides detailed thermal information of each layer the heat passes through, from junction to ambient. This enables identification of the physical characteristics of layers such as die attach, base, package, heatsink and even cooling devices such as a fan.

With this method, engineers are now able to identify the die-attach failures of single-die packages⁴, produce a dynamic compact model of cooling mounts for faster board-level design⁵, conduct thermal reliability tests for an LED package⁶, and even evaluate the thermal performance at the system level, such as a laptop computer or laser printer. The mathematics behind the transformation of the temperature versus time curve into structure functions is described in the appendix.

Examples of structure function applications: Characterizing interface resistances

Some portions of an LED package are highly stable (for example, the chip, submount, heat slug) However, the thermal interface material (TIM) layers, which are applied to fill the small gaps between attachment surfaces, can show large variation even in samples from the same manufacturing lot. Testing the TIM itself yields no hint on the actual thermal resistance achieved in the fabricated TIM layer. These unavoidable variations in the product can be best studied using structure functions.

Figure 1 shows the typical thermal interfaces in an LED application. Their quality can be measured as the length along the thermal resistance axis as shown in figure 2. There could be many reasons why interfacial thermal resistance changes: curing/soldering temperature change, variation in the thickness of the TIM layer, aging, or the quality is changed on purpose.

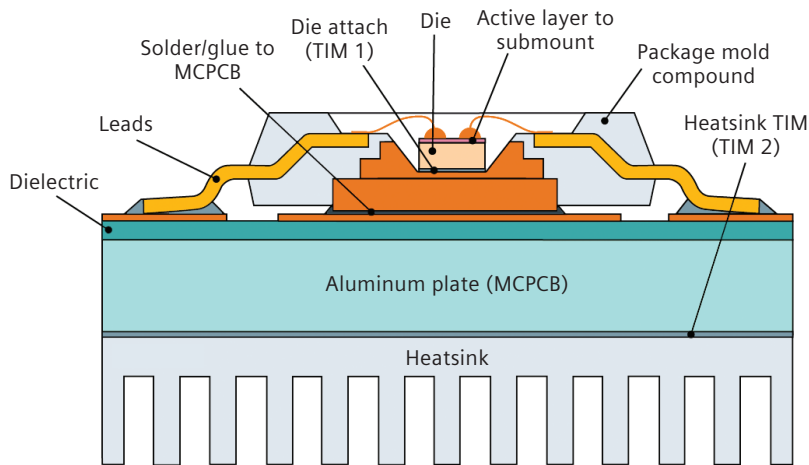


Figure 1: Different thermal interfaces in the junction-to-ambient heat-flow path of a typical LED application.

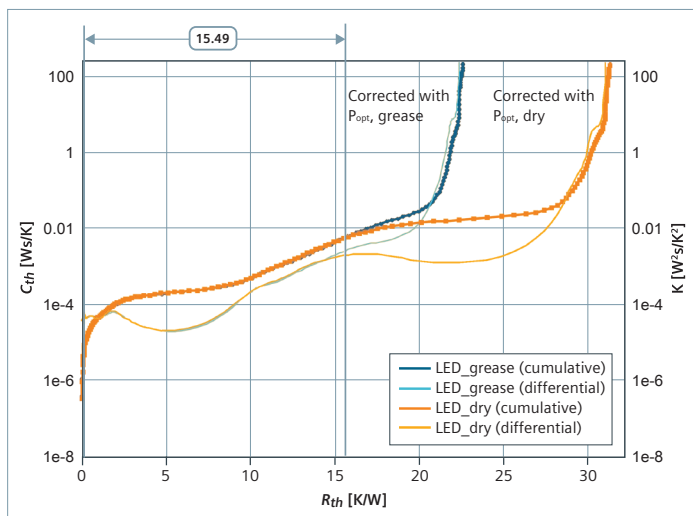


Figure 2: Differential (thin line) and cumulative (thick line) structure functions, for an LED component. R_{th} based on heating power (power corrected for light output)¹.

Measuring interface material thermal conductivity

In the setup shown in figure 3, the $\Delta T_j(t)$ junction temperature transient of the power diode is measured at a well-specified, preset thickness of the material (bond-line thickness, BLT). As the power diode heats up, the heat generated passes through the sample into the cold plate below.

As the sample thickness is changed with a precise, dedicated mechanical system, the total measured thermal impedance of the complete test setup will change. The structure functions in figure 4 show that the change of the total junction-to-cold plate resistance of the test setup was caused solely by the changes in material sample thickness. The thermal behavior of the power diode can be seen to be unchanged, as are the interfacial resistances on either side of the sample under test.

The λ thermal conductivity of the sample can be calculated as follows:

$$\lambda = \frac{1}{A} \times \frac{\Delta L}{\Delta R_{th}}$$

where A is the cross-sectional area of the heat flow path across the sample, ΔL is the bondline thickness change, and ΔR_{th} is the corresponding change in the total thermal resistance of the test setup.

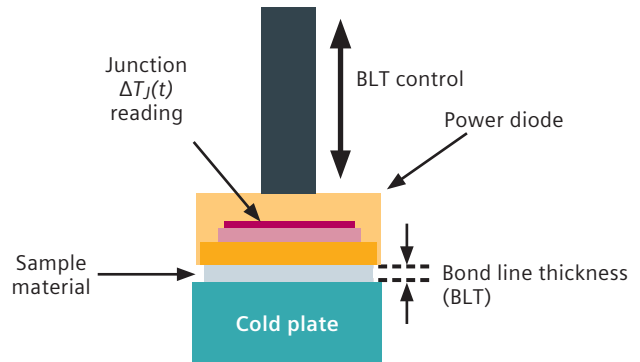


Figure 3: Dynamic TIM testing setup based on junction temperature transient measurements¹.

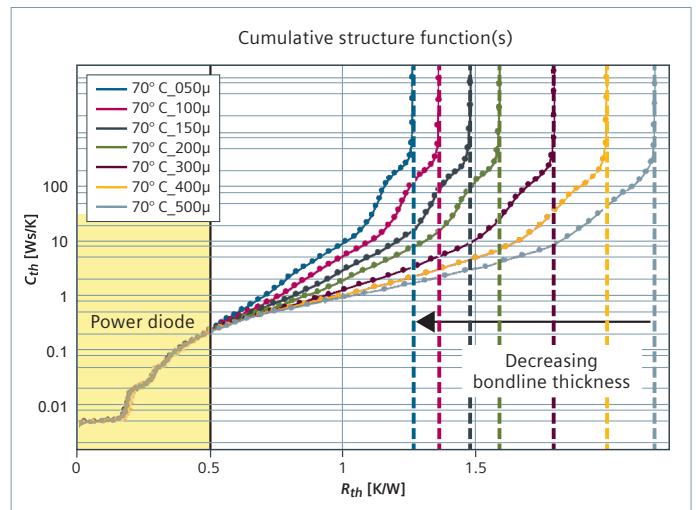


Figure 4: Structure functions of the dynamic TIM testing setup measured at different preset bondline thicknesses of the material tested¹.

According to the equation, the thermal conductivity of the TIM sample tested is directly proportional to the slope of the R_{th} -BLT diagram obtained for the sample (figure 5).

There are some advantages of this TIM testing method compared to other techniques. For example, measurement uncertainty is reduced by the differential approach. The test method is a quasi in-situ technique because the test fixture resembles the real-life application conditions of TIM materials. Last but not least, every measurement includes an inherent self-test of the measuring system. Based on the obtained structure functions, the structural integrity of the test fixture can always be checked. This approach is implemented in the Simcenter DYN-TIM™ software⁸, which automatically performs TIM testing with transient thermal analysis using the structure-function method.

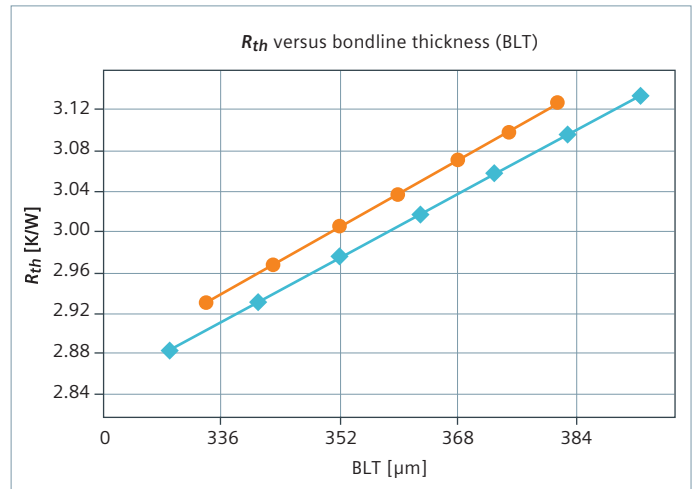


Figure 5: Thermal resistance versus bondline thickness plots obtained for a given material type measured in a dynamic TIM testing setup shown in figure 3¹.

Improving thermal model accuracy through calibration

A simulation model is only as good as the available input data, that is, the device geometry and material properties. This is always an issue when creating detailed models for a computational fluid dynamics (CFD) simulation tool, even for semiconductor vendors who in principle must be aware of at least the device geometry. But many times, material parameters and effective volumes or area raise questions. As noted, a possible source of uncertainty in detailed thermal simulation models is the interface thermal resistance, both at TIM1 (die attach) and TIM2 (for example, thermal grease).

The idea behind using structure functions for detailed model calibration/validation is that if both the geometry/material properties in the simulation model and the boundary conditions correspond to the real-life situation, then there should be no differences between the measured and simulated thermal-impedance curves. Any small difference caused by geometry or material mismatch should, therefore, be visible in the corresponding structure functions.

The following case study shows how a power semiconductor device package model could be fine-tuned with the help of structure functions⁹: creating the calibrated detailed model of BD-242-type transistor housed in a TO-220 package.

Figures 6 through 8 show the major iteration steps taken to adjust the simulation model. In the early iteration steps, the die size and the area of the active (dissipating) chip-surface region were matched. With this modification, the first section of the heat-flow-path model was corrected (figure 6). The match between the simulated thermal impedance and the measured thermal impedance was perfect up to a cumulative thermal resistance value of approximately 2.5 K/W.

After the die-attach layer's properties were also modified (interface resistance set to the proper value by adjusting the thermal conductivity of the TIM1 material), the matching of the structure functions was perfect up to roughly 4.4 K/W (figure 7).

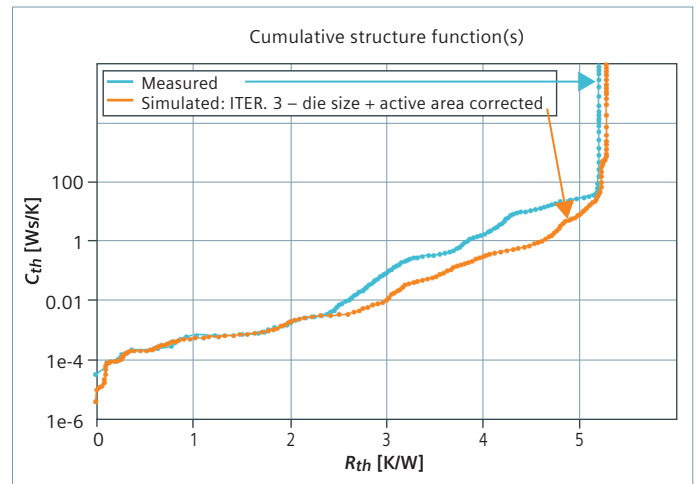


Figure 6: Correction of the die size and the area of the active (dissipating) region⁹.

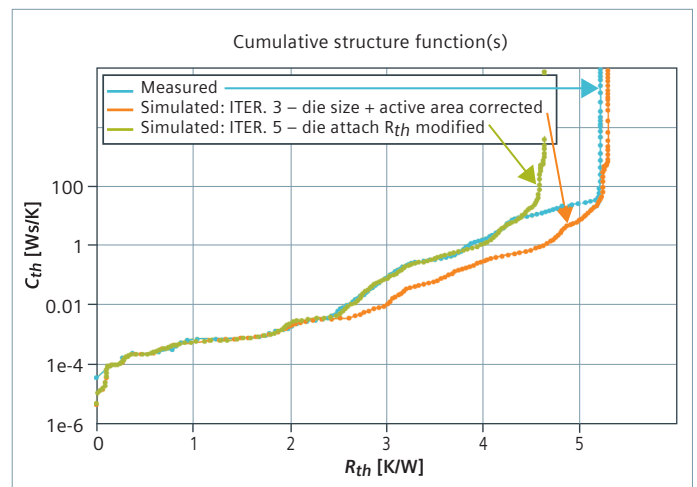


Figure 7: Die-attach thermal resistance also corrected⁹.

The last step in the model calibration was to properly set the thermal resistance of the applied TIM2 layer (figure 8). Thus, the model calibration was completed. The remaining difference was attributed to the modeling of the cold plate that was used.

This procedure can be done automatically using the CFD simulation tool, Simcenter Flotherm™ software command center, which uses data from the Simcenter T3STER transient thermal tester.

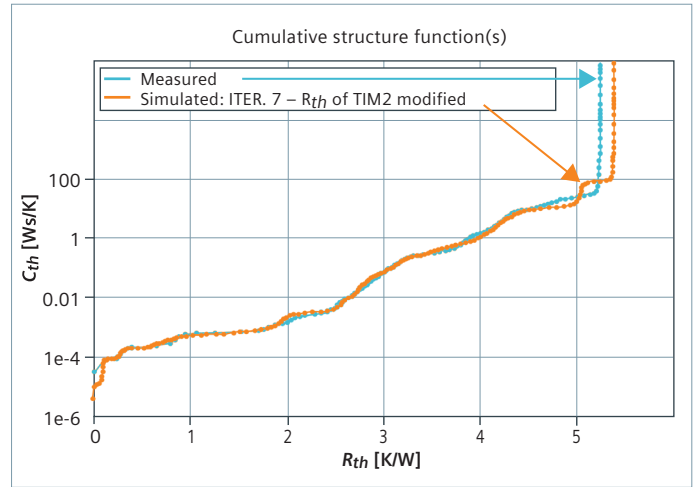


Figure 8: Final calibrated model with adjusted TIM2 thermal resistance⁹.

Conclusion

Just two examples were discussed on how structure functions can be used to analyze what is happening thermally inside a semiconductor package, or any complex electronic system for that matter. Structure functions also can be used for other applications such as to obtain thermal measurements in multichip packages, to conduct in-situ testing of TIMs in a package under different environmental conditions, to provide data for reliability analysis using temperature and power cycling, and to test AC-driving LEDs.

These capabilities are available today in testing equipment by the Simcenter T3STER thermal transient analysis system, Simcenter TERALED™ software for analyzing LEDs, Simcenter DYNTIM for testing TIMs and the Simcenter POWERTESTER™ 1500A software for power cycling and testing packages in the lab or on the factory floor.

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Appendix: The math behind cumulative and differential structure functions

Structure functions are obtained by direct mathematical transformations from the measured or simulated thermal transient response functions of the system. They are a “graphical” representation of the RC model of a thermal system. In the case of essentially 1D heat-flow (such as longitudinal flow in a rod, or radial spreading in homogeneous material layers, or even in cylindrical or spherical spreading), structure functions can be considered as direct models of the thermal system.

Cauer-equivalent models of thermal impedances also can be generated from the time-constant spectra (for more details and theory behind this, see *Thermal Management for LED Applications*¹).

The practical problem with such a network model is that 150-200 individual thermal resistance and thermal capacitance values cannot be interpreted. But by introducing two simple definitions, the Cauer-equivalent model can then be represented graphically. The cumulative thermal resistance is defined as the thermal resistance between the n -th element of the model network and the heat source (driving point)⁷:

$$R_{\Sigma} = \sum_{i=1}^n R_i$$

and the cumulative thermal capacitance is

$$C_{\Sigma} = \sum_{i=1}^n C_i$$

where R_i and C_i denote the element values of the i -th stage of the Cauer-type model network.

Starting from the driving point (the junction heat source), the sum of the partial thermal resistance and partial thermal capacitance values for all subsequent heat-flow-path sections can be calculated.

Interpreting the cumulative thermal capacitance as a function of the cumulative thermal resistance, the so-called cumulative structure function (CSF) is obtained:

$$CSF = C_{th\Sigma}(R_{th\Sigma})$$

It can then be proved that the derivative of $C_{\Sigma}(R_{\Sigma})$, the differential structure function, $k = dC_{\Sigma}/dR_{\Sigma}$, is proportional to the square of the cross-sectional area of the conducting path. Cauer ladders are obtained from Foster models¹ that are directly calculated from the discretized time constant spectrum of the thermal system.

The origin of the function corresponds to the junction. Because all thermal capacitance values are positive, it follows that the cumulative structure function should be a monotonically increasing function. The heat-conduction path ends in the ambient, which has an infinite heat sinking capacity; therefore, the cumulative thermal capacitance must tend to infinity. This means that the cumulative structure function should end with a singularity (at the location corresponding to the ambient). As a further consequence, the distance between the singularity and the origin is the junction-to-ambient thermal resistance (R_{thJA}).

If there is heat flow through a small portion of material, two effects can be observed.

The first effect is a temperature drop between two (isothermal) surfaces of the material (assuming an adiabatic condition at the other four faces of the cuboid).

If the material has thermal conductivity (λ) and power (P) flows through the surfaces a and b , they will have T_a and T_b temperatures, measured from the ambient. So, if the slice has a small length (dx) and a surface with cross-sectional area (A), then the temperature drop between the two sides can be expressed as:

$$T_a - T_b = P \left(\frac{1}{\lambda} \frac{dx}{A} \right)$$

where the expression in the bracket on the right side is the R_{th} thermal resistance between the a and b points corresponding to the two surfaces:

$$R_{th} = \left(\frac{1}{\lambda} \frac{dx}{A} \right)$$

The second effect arises because the same material slice can store thermal energy. If there is heat flow into the material, then in a short $dt = t_2 - t_1$ time interval the energy change is $dQ = Pdt = C_{th}(T_2 - T_1)$, if $T_1 = T(t_1)$ is the temperature of the material at t_1 time and $T_2 = T(t_2)$ is the temperature of the material at t_2 time.

Now, the slice can be represented by a single point for the simplest approach. As T_1 and T_2 temperatures are again measured from the ambient, the following equation defines a thermal capacitance (C_{th}) between a point representing the material portion and the ambient. The value of this C_{th} thermal capacitance can also be expressed through material parameters: $C_{th} = cm = \rho dx A$ or $C_{th} = c_v V = c_v dx A$, where c denotes specific heat capacity, m denotes mass, ρ is the density, c_v denotes volumetric (specific) heat capacity, and V denotes volume.

How to interpret the results

The cumulative structure function is a graphic tool that has proven to be useful for analyzing physical structure.

In low-gradient sections, it shows that a small amount of material with low capacitance is causing a large change in thermal resistance. These regions have low thermal conductivity and/or small cross-sectional area.

Steep sections correspond to material regions of high thermal conductivity or large cross-sectional area. Sudden breaks of the slope belong to material or geometry changes. In such a way, thermal resistance and capacitance values, geometrical dimensions, heat-transfer coefficients and material parameters can be indirectly interpreted from cumulative structure functions.

In a real environment, the heat flow can have various shapes – longitudinal along a beam, radial in a board, or conical in a heatsink below a smaller package. In most cases, a “proper” slicing of the material can be made on the isothermal surfaces, perpendicular to the direction of the flow. These slices must be narrow, but not always of a very small cross-sectional area (figure A1), and the surfaces are usually not planes.

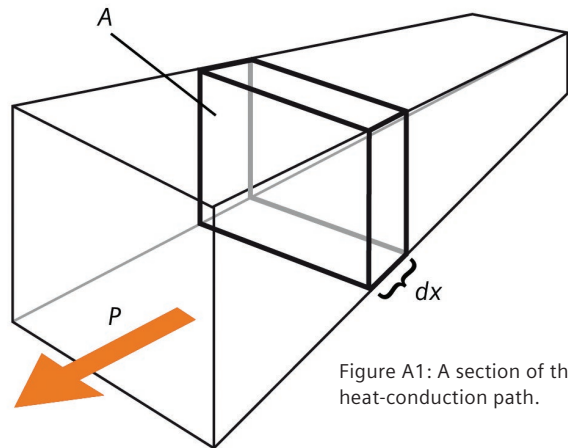


Figure A1: A section of the heat-conduction path.

It is sometimes easier to identify the interface between the sections using the derivative of the cumulative curve, known as the differential structure function (DSF). Here, peaks correspond to regions of high thermal conductivity, such as the chip or a heatsink, and valleys show regions of low thermal conductivity, such as the die attach or air. Interface surfaces are represented as inflexion points between peaks and valleys.

The differential structure function, derived from the previous two equations, also yields information on the cross-sectional area along the heat conduction path:

$$DSF = \frac{dC_{th\Sigma}}{dR_{th\Sigma}} = c_v \times dx \times A \times \left(\frac{1}{\lambda} \frac{dx}{A} \right)^{-1} = c_v \times \lambda \times A^2$$

For example, consider the homogeneous rod with thermal boundary conditions shown in figure A2. This rod can be considered as a series of infinitesimally small material sections. Consequently, the network model of its thermal impedance would also be a series connection of the single RC stages. With this slicing along the heat conduction path, a ladder of lateral thermal resistances is created between two thermal nodes and thermal capacitances between a node and the ambient.

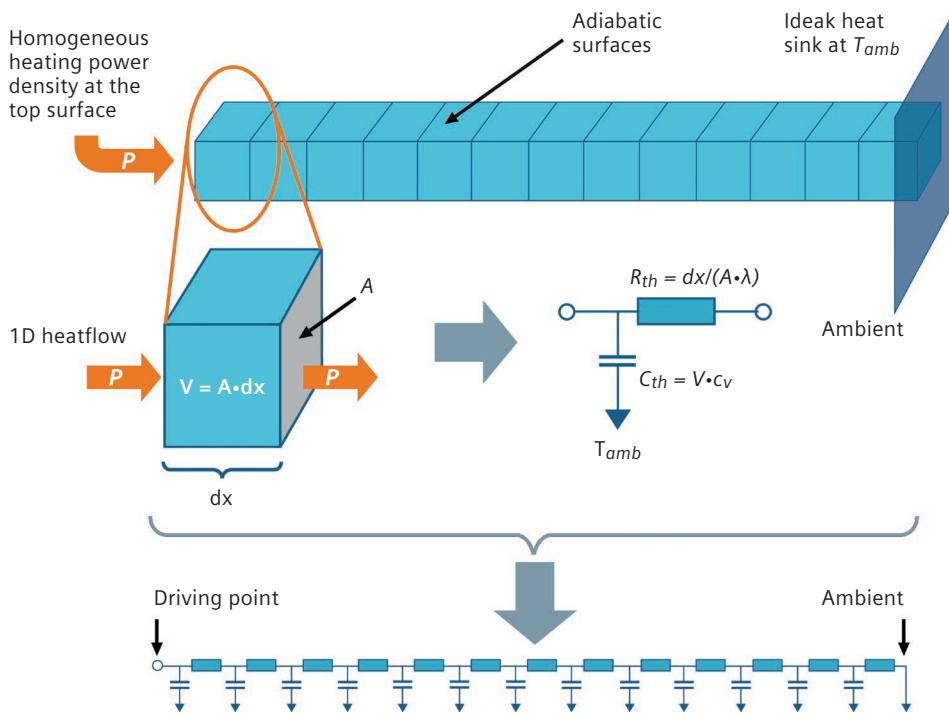


Figure A2: The RC model of a narrow slice of the heat-conduction path with perfect 1D heat flow and the Cauer-type network model of the thermal impedance of the entire heat-flow path¹.

Assuming homogeneity, the ratio of the elementary thermal capacitances and thermal resistances in the network model shown in figure A2 would be constant. As shown in figure A3, this means that the cumulative structure function of the rod would be a straight line – its slope is determined by the C_{th}/R_{th} ratio of the

network model, and its differential structure function would be a constant pn-junction C_{th}/R_{th} ratio of the element values. This example demonstrates that the features of the structure functions are in a one-to-one correspondence with the properties of the heat-conduction path.

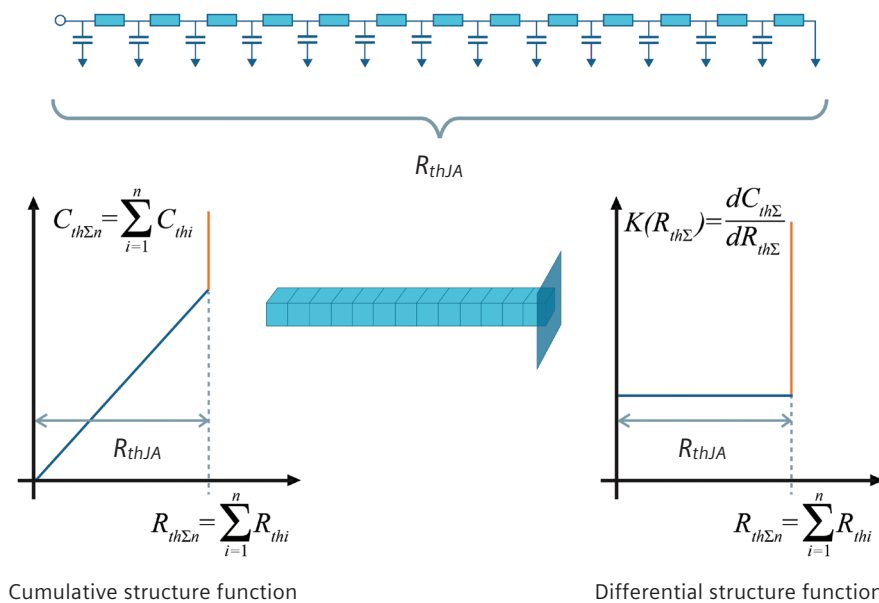


Figure A3: The cumulative and differential structure functions of a homogeneous rod.

Assume that in a given section in the middle of the rod, the C_{th}/R_{th} ratio is halved. As figure A4 shows, this results in a shallower middle section in the cumulative structure function (with the slope halved), and a corresponding dip in the differential structure function (being half the height of the sections either side of it).

Therefore, the differential structure function is a powerful tool for detecting slight changes in the cumulative structure-function curve, aiding the interpretation of the results.

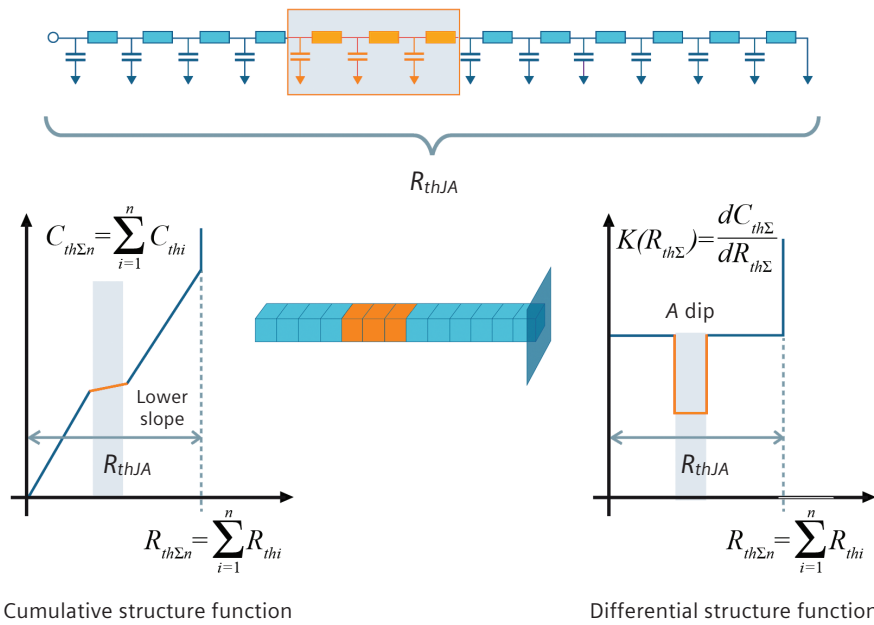


Figure A4: Structure functions indicate the changes in the C_{th}/R_{th} ratio along the heat-conduction path.

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