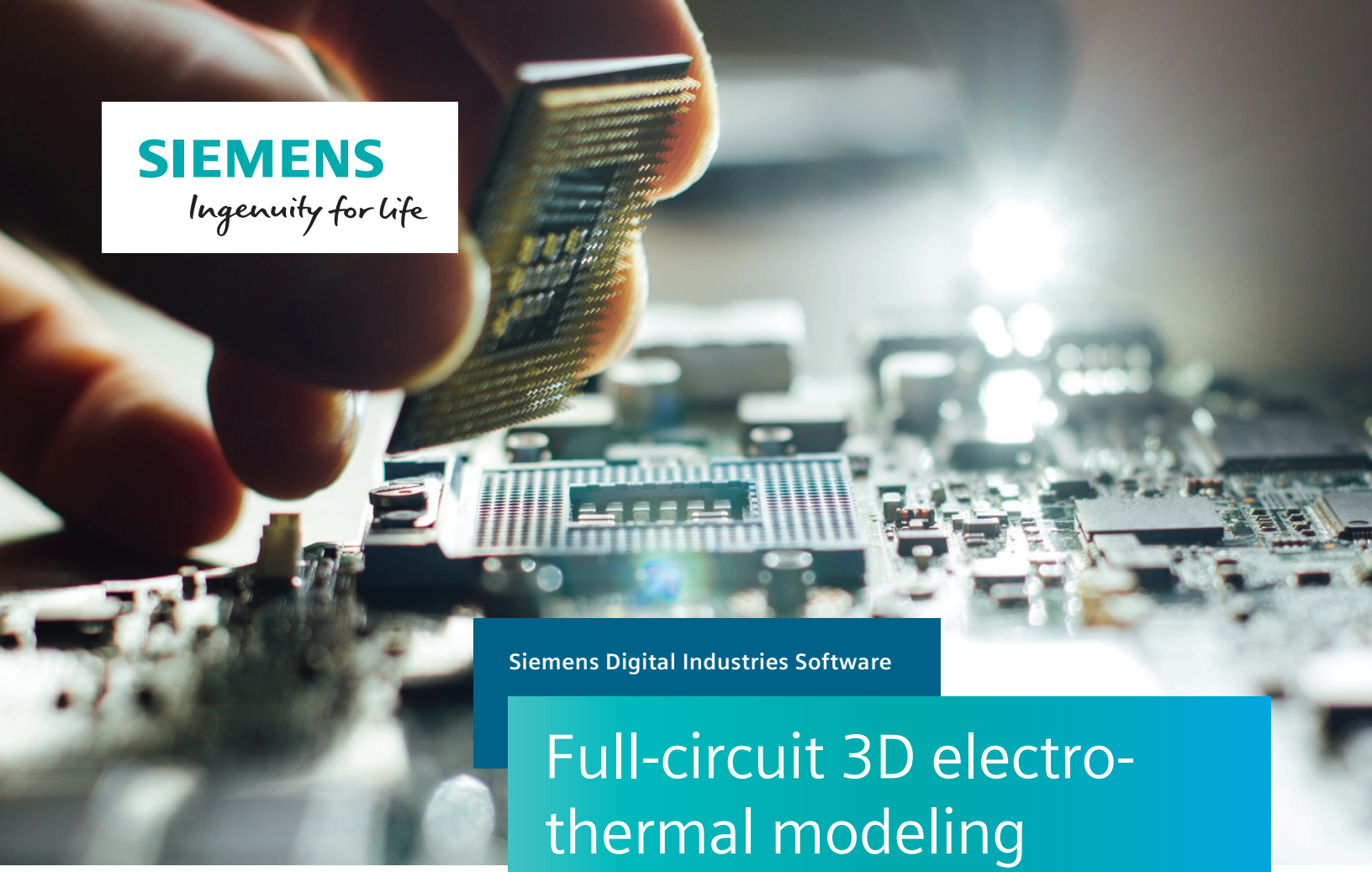

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Full-circuit 3D electro-thermal modeling

Achieve higher accuracy with measurement and calibration

Executive summary

The 3D thermal simulation of electronics systems typically assumes that all power is dissipated in the semiconductor with the value of power being prescribed. In the case of high-current power modules, the power dissipation in the electrical distribution network has become a significant factor. In commercially available components, the power dissipation in the copper traces can be in the range of 30 percent of total input power. This tendency makes it essential to consider this heating effect in the simulation because considering semiconductors as the only heat source may not be an accurate approach for current high-end and future applications.

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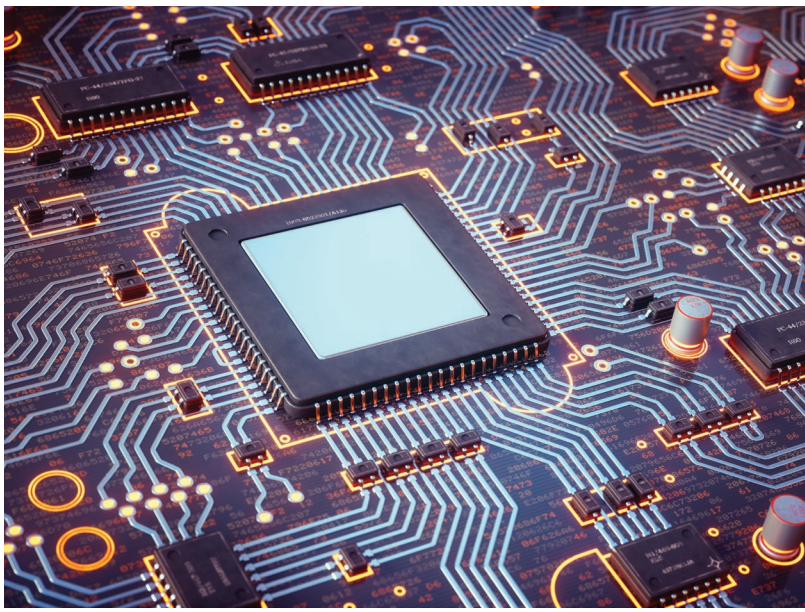
Abstract

The power dissipation value, and the assumption it is dissipated solely in the semiconductor, can result in substantial errors in temperature-rise predictions. These errors can be overcome by using an electrothermal simulation approach in which the full electrical circuit is simulated, predicting the resistive heating in the power delivery network as well as the dissipation in the semiconductor. Solving for both the electric and thermal behavior of a system allows for power levels and distribution to be predicted, thus improving temperature-rise prediction accuracy.

This article describes the method using an insulated-gate bipolar transistor (IGBT) power inverter as an example. The resulting full-circuit electrothermal simulation predicts power dissipation and temperature variation throughout the power-inverter module.



Power dissipation distribution affects thermal simulation

The accuracy of a temperature-rise prediction is predicated on the accuracy of the power dissipation in terms of magnitude and distribution. A common assumption is that power is only dissipated in the active layer of the semiconductor chip. But for high-current-power electronic applications, an appreciable amount of power is dissipated in the rest of the power delivery system. As the trend of decreasing drain-source on resistance (Rds (on)) continues, the relative electrical resistivity, thus power dissipation, of the power delivery system will become increasingly significant. How can this trend be accommodated by simulation?

Evaluating electrothermal simulation approaches

An IGBT is a three-terminal power semiconductor device primarily used as an electronic switch that combines high efficiency and fast switching. Circuits with IGBTs can be developed and modeled with various circuit simulating computer programs, such as SPICE and Saber. To simulate an IGBT circuit, the device (and other devices in the circuit) must have a model that predicts or simulates the devices' response to various voltages and currents on their electrical terminals. For more precise simulations, the effect of temperature on various parts of the IGBT may be included with the simulation.

Power can be predicted, potentially for the temperature dependence of the power, by solving for both the electric and thermal behavior of a system. This is usually done using one of two standard approaches. The relaxation method couples two independent electro and thermal solvers, passing temperature and power between them. The direct method solves for both electro and thermal behaviors in a single solver. Electrothermal SPICE-type network solvers that use the direct method are becoming common.

We conducted a study to investigate how well the direct method works in the context of a full 3D electrothermal simulation. The aim of the study was to verify the accuracy of the simulation model in predicting the power dissipation distribution and the resulting variations in temperature increase.

Taking real measurements of the IGBT

We first ran an Infineon FS800R07A2E3 IGBT power-inverter module in the lab through Simcenter T3STER™, which can be used to get accurate measurements of what is happening inside the chips.

The module contained three half-bridge stages, and we selected the third phase's low-side IGBT for testing. The power in the IGBT was distributed between two identical chips for better power management. The component was tested in saturation mode; that is, we applied voltage through a 15 volt (V) gate to open up the device and switched between 500 amps (A) heating and 500 milliamps (mA) sensor current to initiate a good power step on the semiconductor component.

The sample had powering terminals for the high current (called 3 and N3), and also separate sensor terminals (called C6 and E6) connected to the emitter and the connector of the IGBT individually. These separate sensor terminals allowed us to create a true Kelvin-probe setup, in which the powering and the measurement lines were separated for the more accurate voltage drop measurement over the chip.

We assumed the voltage drop on the metallization could significantly affect the results of the thermal transient tests. So to check this, we tested the thermal resistance of the sample by powering and sensing on the main power pins (3-N3) and then powering on pins 3-N3, while sensing on the dedicated sensor pins, C6-E6. Because the temperature sensitivity of the system primarily depends on the tested semiconductor, in both cases the measured temperature responses were the same. However, if we considered the internal metallization in our measurement, we got approximately 900 watts (W) heating power, but only 700 W if we directly measured on the semiconductor.

The location of the measurement pins also heavily influences the calculated structure functions, or the measured thermal resistances. To verify the effect, we created an accurate 3D electrothermal model of the setup and analyzed it.

Tuning and calibrating the model

An accurate, steady-state, 3D electrothermal model requires well-defined electrical and thermal resistance properties, which means the geometry, electrical resistivity and thermal conductivity values have to be determined and precisely described. To achieve this, we tuned the 3D electrothermal model against a combination of the measured chip temperature, the chip's transient temperature response to a unit power step (Z_{th} curve), and point voltage drops. We applied a 500-A boundary condition at Pin N3, 0V at pin 3, and used Pin E6 and C6 to monitor the voltage drop over the IGBT chips.

The stackup section through one of the active IGBTs is shown in figure 1. The model provided a sufficiently detailed representation, including the chip metallization, active layer, chip, solder, direct copper bond (DCB) substrate, etc. We designated all inactive IGBT and diode active layers, as well as the ceramic layer as dielectric, isolating the electrical circuit to the power delivery network, metallization layers, bond wires and the chip and active layers of the two active IGBTs.

The IGBT module had an integrated pin-fin heat sink at the bottom of the baseplate, cooled by a water jacket. We didn't model the pins and water jacket explicitly. Instead, we defined a contact thermal resistance at the bottom of the baseplate, between it and a fixed temperature boundary condition over the area of the baseplate where the fins were located. The electrical resistivity material properties of all the metallic objects were well-characterized, including temperature-dependent coefficients.

The two main unknowns were the electrical resistivity of the active layer and that of the doped silicone-based chip. The former was the most sensitive parameter and formed the basis of the calibration. For the latter, the value was dependent on dopant concentration, though it was much smaller than that of the active layer, thus it was less sensitive. We assumed a value of 2e-5 Ohm m.

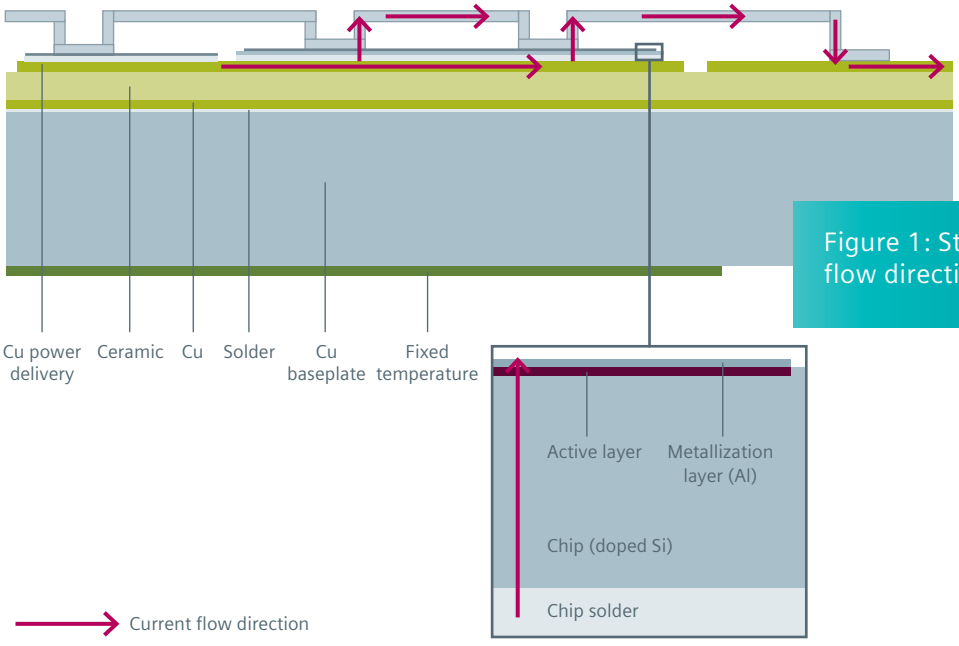


Figure 1: Stackup and current flow direction.

When analyzing thermal conductivity material properties, the two values found to be most sensitive to the predicted temperature rises were the ceramic and the contact resistance representing the pin fins that had not been modeled. So our calibration procedure involved varying the active layer electrical resistivity, the ceramic thermal conductivity and thickness, and the contact resistance at the fixed temperature boundary condition. We varied the parameters until our T3STER measurements for the two measured voltage drops (N3-0 and E6-C6), average steady-state chip temperatures, and Z_{th} and the cumulative structure functions were replicated by the 3D model in Simcenter Flotherm™ software.

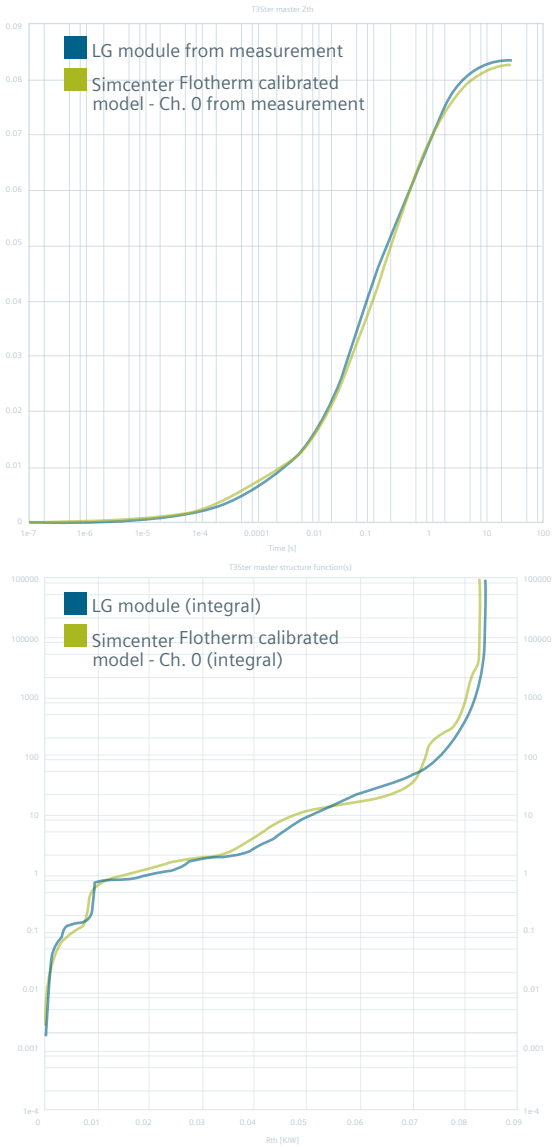


Figure 2: Z_{th} and cumulative structure function calibration comparison.

For our final calibration, we set the ceramic layer at 740 microns thick with a thermal conductivity of 105 watts (W)/per meter Kelvin (mK), the effective electrical resistivity of the active IGBT layer at 0.115 Ohm-m, and the contact resistance representing the pins and water jacket at 3.5e-5 meter squared Kelvin (m^2K)/per watt (W). Although it was possible to take measurements of all accessible geometry, we made no destructive, sectioning measurements. So the exact values of the effective resistivity of the active layer and thermal conductivity and (ceramic) thickness might not be exact; however, the resulting effective electrical and thermal resistances were calibrated (table 1).

To simulate the transient temperature response to an increase in power of the system (Z_{th}), we used the same approach when performing the T3STER measurement. Starting from a driving-current, steady-state, electrothermal solution at t = 0 s, we conducted a transient thermal-only simulation and recorded the resulting chip average temperature versus time curve (figure 2). Although in reality, T3STER switches down to a sensing current at the start of the transient measurement, such currents are low enough that our assumption of no self-heating was valid.

Although the calibration against a transient thermal response measurement does in theory calibrate the model for transient thermal behavior, our intention was to further confirm the thermal material properties outside of the IGBT. This was to ensure that the predicted steady-state temperature rise was correct for the right reasons, not as a consequence of the summation of erroneous thermal resistances in the stack leading to a coincidentally correct overall thermal resistance (R_{th}). This approach helped us to ensure correct temperature prediction through the stack, not just chip temperatures.

What we learned about power dissipation

Under low current conditions (such as sensing), the electrical resistivity of the IGBT was far greater than the rest of the circuit. The vast majority of the dissipated power occurred at the chip. At high currents, the relative resistivity of the chip decreased with respect to the rest of the circuit, and the assumption that all the consumed power was dissipated at the chip was incorrect. The simulated power budget at the driving current of 500 A is shown in figure 3.

Out of the total consumed power of 912 W, 64 percent was dissipated on the active layers of the two IGBTs, 4.7 percent in the bond wires, 1.4 percent in the metallization layers, and the remaining 29.6 percent in the rest of the power delivery circuit. The ratio of the voltage measurements at the four pins, N3-0 covering the entire circuit, E6-P6 covering the IGBT chips and bond wires, 1.4/1.812 V = 77 percent, provided us with a first-order indication of the power budget split between the active devices and the power delivery circuit.

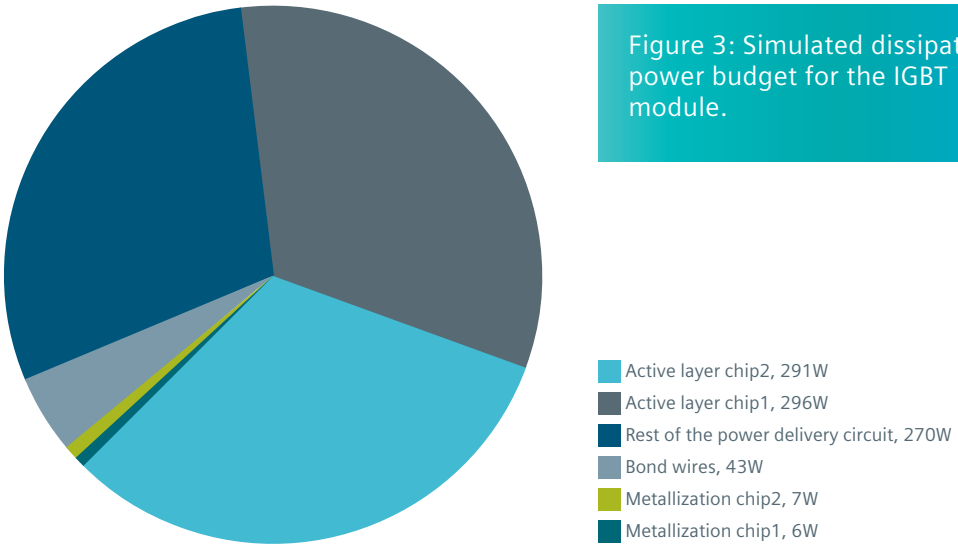


Figure 3: Simulated dissipated power budget for the IGBT module.

Effects on power distribution in the active layer

For the current flowing up through the active layer, the effectiveness of the metallization layer in spreading the current to the attached bond wires, as well as the proximity of the bond wires to the return part of the power delivery circuit, determined the distribution of current and thus the distribution of power within the active layer. The nonuniformity of the current being carried by each bond wire is shown in figure 4.

Bond wires nearer the 0-V return pin (top left) carried approximately 20 percent more current than those furthest from the return (top right). We assumed this because of the reduced electrical resistance between the bond wires closer to the 0-V return compared to those further away.

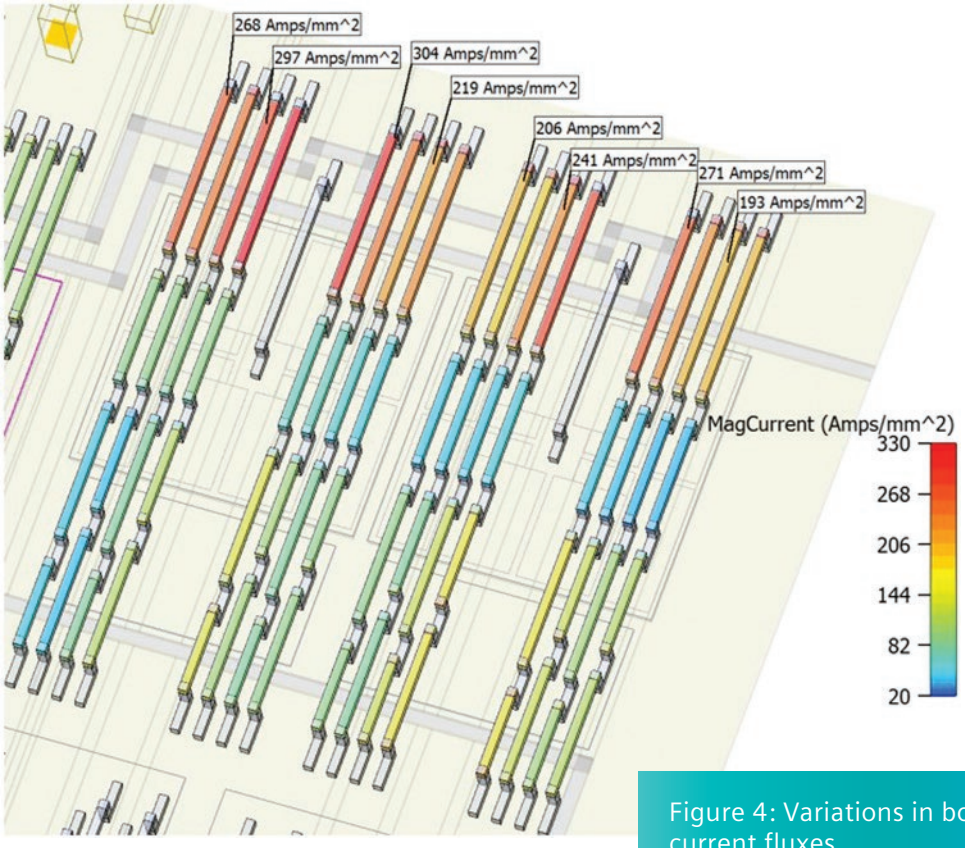


Figure 4: Variations in bond wire current fluxes.

Comparing assumed total power dissipation in chip

A thermal-only simulation would consist of an estimate of the power dissipation and its location. The total power dissipation can be determined by measuring the voltage drop over the whole circuit and multiplying that with the known current. However, assuming all the consumed power was dissipated in the active layer and dissipation was uniformly distributed, this would result in considerable temperature prediction errors (figure 5). As shown here, this assumption results in the maximum temperature rise predicted at 34 percent higher, the location of the maximum temperature at a different point, and the temperature variation across the active layer as 30 percent greater.

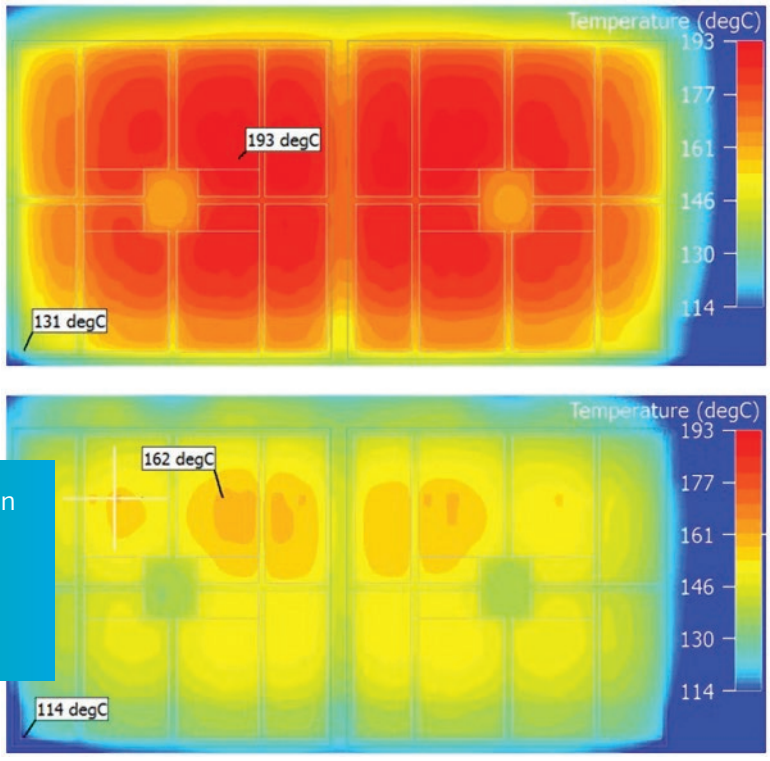


Figure 5: Temperature prediction with full power uniformly dissipated (top) and with an electrothermal approach (bottom).

Limitations of using a linear electrical model

Because a single electrical resistivity material property is assumed in Simcenter Flotherm, whereas the IGBT exhibits a nonlinear IV relationship, calibrating to a single driving current inside a device such as an IGBT is limited when using simulation only. Although such a resistivity can be (linearly) temperature dependent, it limits the general application to materials that exhibit a linear, through origin, IV characteristic. The total power dissipation is readily measureable (full-circuit voltage drop measurement in conjunction with knowledge of the driving current). The calibration methodology determines the (electrical) operating point by adjusting the active layer resistivity contribution so as to intersect the IV curve with the driving current line (figure 6).

Calibrating the active layer's effective electrical resistivity but at the same driving current and at differing junction temperatures (via control of the ambient water jacket temperature) would enable the temperature-dependent coefficient of that electrical resistivity to be determined. This also might refine the accuracy of predicting power dissipation of the active layer, taking into account local variations in chip temperature and electrical resistivity. A more generalized electrical material property defined by an I versus V versus T characterized surface would allow for the full range of operating currents to be handled in simulation, including temperature dependency.

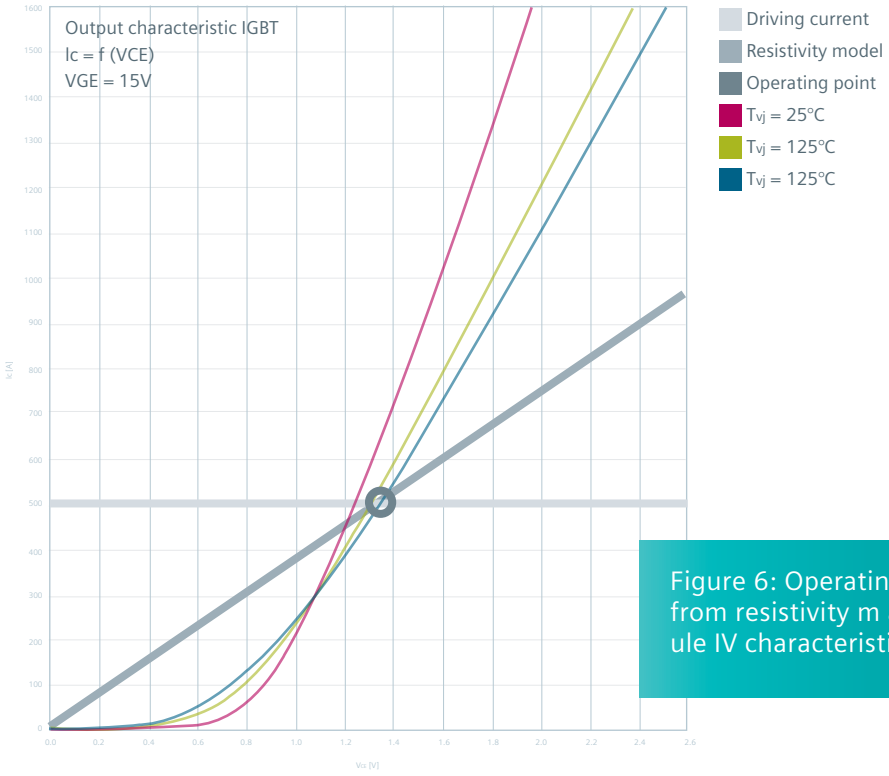


Figure 6: Operating point derived from resistivity m and IGBT module IV characteristic intersection.

Overcoming the limitations of modeling total power dissipation during switching

When the IGBT module is in operation, the total power dissipation is comprised of a contribution from the DC losses and the losses that occur during switching. From a 3D transient modeling perspective, it is not tractable to consider resolving electrical switching timescales concurrently with the thermal timescales of the rest of the system.

An alternative approach would be to use a circuit simulator such as ELDO to perform a full transient electrical stimulation. From the predicted instantaneous power profile, the DC contribution would be subtracted, leaving the switching loss profile. That could then be time-averaged to derive the cumulative switching loss power. This value could then be implemented as a steady-state power source, collocated with the active layer objects in the 3D electrothermal model, thus allowing the time-averaged switching losses to be considered in addition to the electrothermally predicted DC losses.

Conclusion

Legacy thermal simulation approaches that assume all consumed power is dissipated in the semiconductor can lead to 34 percent more errors in temperature-rise predictions for such power electronics applications. Solving the full electrical circuit on a T3STER calibrated Simcenter Flotherm simulation model enables the distribution of power to be predicted, which leads to highly accurate temperature-rise predictions that can be used to judge the thermal compliance of a proposed design under operating conditions. This combined test and simulation methodology can be used to contribute to the accuracy of a digital twin.

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